POWER-EFFICIENT SEMICONDUCTOR DESIGN

Power budgeting solutions that manage full-chip power consumption and integrity are required to develop modern electronic devices, cars and data centers with high-fidelity tools.

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Today's electronics require power efficiency.

If you read the latest consumer electronics reviews, you'll readily see how these modern devices are entrenched in our society, and why power is at the forefront of semiconductor designs. From smartphone to tablet to laptop to GPS device to MP3 player, the incredible capabilities of these devices drive consumer demand that, in turn, drives low-power integrated circuit (IC) designs.

However, it isn't just hand-held devices that are directing the power efficiency of IC design and manufacturing. Cars today have dozens of microprocessors, and the increasing power consumption of onboard automotive electronics is forcing manufacturers to consider 48-volt systems. Likewise, today's data centers have an insatiable demand for power. Massive telecommunications connections and storage systems with redundant backup power supplies, environmental controls and security devices also require a tremendous amount of power.

Power-efficient design is not limited to lowering power. The phenomenal growth in device integration and advanced low-power design increases the complexity of ensuring power and thermal integrity of a system-on-chip (SoC). Low-power design techniques such as clock-gating and power-gating result in large power gradients — surges that can cause the power delivery network (PDN) to fail. PDN integrity on a chip, on the board and in the system must be preserved under a multitude of complex functional scenarios.

As power-efficient designs drive the competitiveness of electronic products, the semiconductor industry is re-evaluating its tools and methodologies to meet stringent power requirements. An emerging power-budgeting flow takes a holistic approach to early management of power consumption and power integrity that spans the entire chip design process, from early prototyping to final

system sign-off. This change in methodology is critical to ensure that end-products meet their power specifications (or budgeting limits), performance, cost and reliability targets.

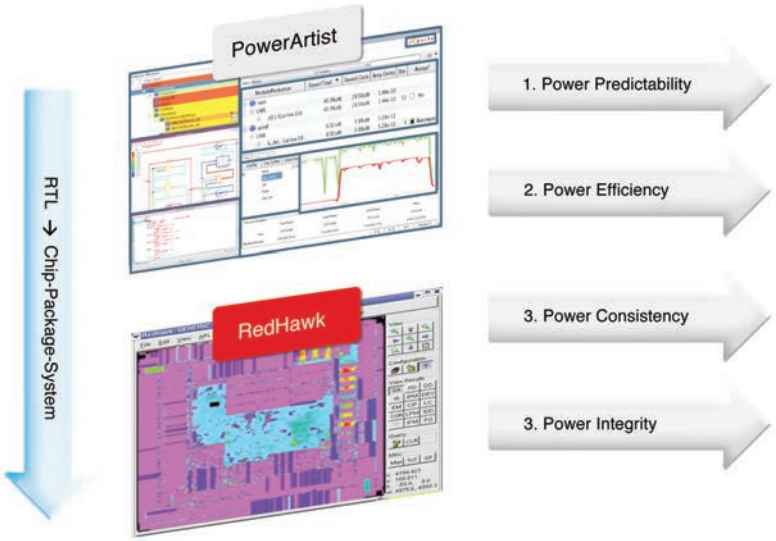
ENABLING PREDICTABLE POWER BUDGETING: RTL POWER MODEL

Leading the way with innovative power management solutions for IC designs, ANSYS subsidiary Apache Design recently launched PowerArtist RTL Power Model (RPM) technology designed to optimize a wide range of power-sensitive electronics applications. RPM accurately predicts a chip's power behavior very early in the design process at the register-transfer-language (RTL) level with consideration for its physical implementation. RPM bridges the gap between the RTL and physical design stages. This allows much earlier chip planning, PDN and IC package design decisions that facilitate predictable power-budgeting, cost reduction and faster time to market for advanced semiconductor applications.

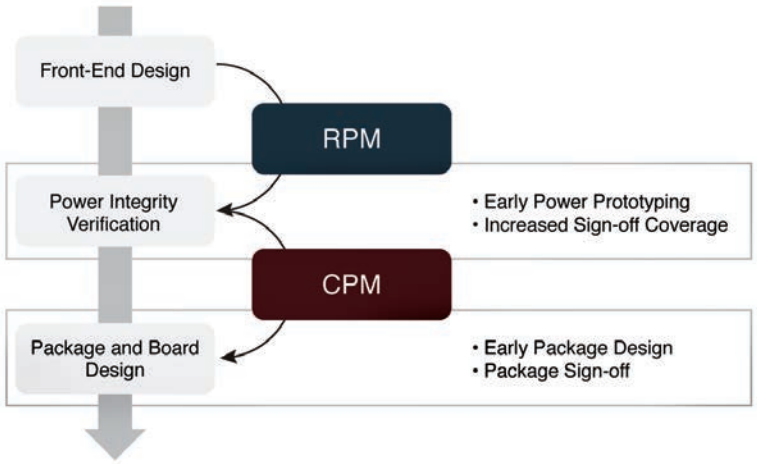
Because of extensive ultra-low power requirements and shortened design cycles, early and accurate predictions are critical to design engineers understanding the IC's power consumption profile as a function of various operating modes, including stand-by, web browsing and video streaming, for example. Such understanding directs a designer's power reduction efforts, which include making architectural trade-offs and identifying power bugs (wasted power conditions that are otherwise functionally correct). Early power estimates also enable early PDN prototyping, which minimizes over- or under-designing a chip.

HOW RPM TECHNOLOGY WORKS

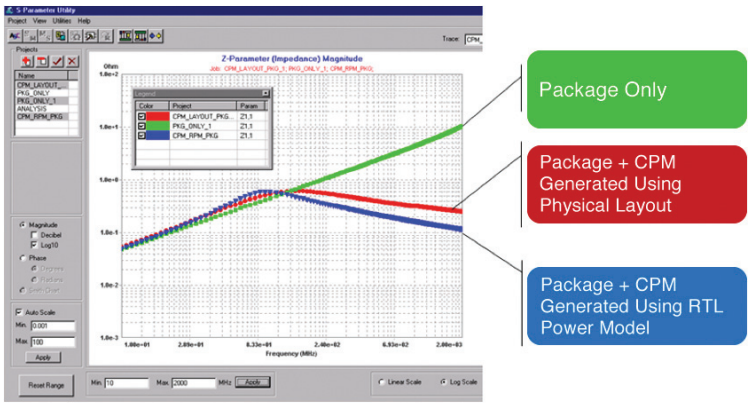
RPM is enabled by, and works in combination with, Apache's portfolio of products including PowerArtist, RedHawk, Chip Power Model (CPM) and Sentinel to provide a seamless RTL to physical power methodology for ultra-low power chip design. Utilizing RTL power analysis, PowerArtist generates an RPM for RedHawk, which then identifies areas on the chip with high dynamic voltage drop — well before a chip design layout is available. RedHawk can also create an early CPM representing the full-chip PDN and current profiles in a compact model, enabling early chip–package codesign.



Apache ultra-low power methodology



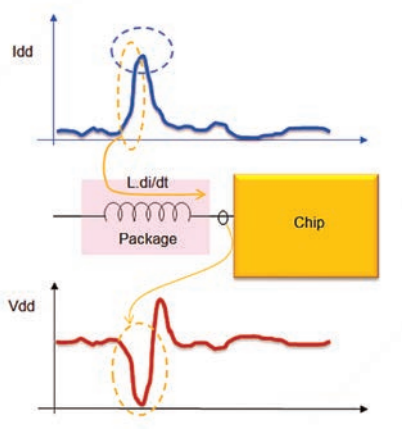
RTL-to-physical power integrity flow using RPM and CPM



Package resonance frequency analysis: tight correlation between RPM vs. layout

By enabling early power analysis, Apache's power-budgeting methodology helps engineers design more power-efficient products that are predictable and reliable.

RPM utilizes information available during the RTL design stage to generate data for early power and PDN prototyping. RPM's key technologies include PowerArtist Calibrator and Estimator (PACE) and Fast-Frame Selector. PACE statistically models physical design parameters to ensure that RTL power estimates are within 15 percent of the implemented design's power consumption. This enables engineers to confidently make timely power-related design decisions, such as the on-chip power grid. Using RPM early in the design flow enables CPM generation, which, in turn, allows package and board designers to perform early chip–package–system codesign to explore system-level implications of power and to make informed package trade-offs. Fast-Frame Selector technology selects a set of the most power-critical cycles to use throughout the design flow, from early design planning to final chip sign-off. It can accurately identify a few cycles representing key power characteristics from millions of RTL simulation vectors within hours, improving productivity and ensuring power sign-off integrity.



Lowering power adds additional PDN integrity challenges. A surge in current causes voltage-induced timing failure.

MANAGING POWER INTEGRITY FOR LOW-POWER DESIGNS

A comprehensive power budgeting solution addresses power analysis and reduction at a high level. It aids in ensuring PDN integrity across power-critical switching scenarios. It helps avoid an underdesigned PDN that can result in power-integrity–related chip failures caused by voltage drop, electromigration, and on- and off-chip reliability issues. It also helps to control overdesign and to manage chip and package costs.

A PDN designed by utilizing power-budgeting flow and RPM early on accounts for a design's worst current demands across increasing operating modes. It eliminates the inadequacy of gate-level simulations that are available too late in the design flow and offer limited coverage. For example, when a clock driving a power-hungry block turns on, there is a sudden surge of current that can couple with the package inductance; this, in turn, can cause a significant voltage drop on the chip and, consequently, a timing failure. The RPM methodology helps to identify such scenarios early and guard against voltage-induced silicon failures.

SMALLER, FASTER, CHEAPER

Most consumers really don't care about the technology behind the latest cool device, they just want it to work well — when they want it and how they want it — at an affordable price. A smartphone that burns your hand, a tablet that must be constantly charged or hearing aids that transmit interference just won't be tolerated. These are the critical challenges that IC designers need to solve for today's low-power market and for the future.

By enabling early power analysis, power reduction and power integrity, Apache's power-budgeting methodology helps engineers design more power-efficient products that are predictable and reliable. This allows companies to be more competitive in a demanding low-power market.